REMARKS/ARGUMENTS

In view of the foregoing amendments and the following remarks, reconsideration of this application is requested. Claims 1-21 are now pending with claims 1, 9, 15, 18, and 21 being independent. Claims 1, 8, 9, 11, 15, 18, and 21 have been amended.

Applicants thank the Examiner for the interview of August 18, 2004. During the interview, the Examiner David J. Huisman and Applicant's representative Indranil Chowdhury discussed claims 1, 5, 9, 15, 18, and 21. The Examiner stated that a new reference Goebel, U.S. Patent 6,131,188, had been found which was relevant to the majority of the independent claims in that Goebel teaches calculating a complete return address in the delay slot of a branch instruction. The Examiner further explained that another new reference Perets, U.S. Patent 6,564,316, had been found which disclosed an instruction that specified a value dictating how many NOP instructions should be executed in the remaining delay slots of an associated branch. The Examiner stated that to overcome both references in combination, applicant should amend the independent claims to include the idea of the branch instruction having multiple delay slots and the instruction which calculates the return address also specifying the number of NOPs to execute in the remaining delay slots. By amending the claims as described above, the Examiner pointed out that Applicants would be better claiming Figure 6A.

Claims 1, 9, 15, and 18 have been amended as requested by the Examiner to overcome the Goebel and Perets references.

Regarding claim 21, the Examiner stated that the claim should be amended to include the idea of a predicate having two states, wherein, when the predicate is in a first state, a first instruction calculates a first return address, and when the predicate is in a second state, a second instruction calculates a second return address. By amending the claims as described above, the Examiner pointed out that Applicants would be better claiming Figure 6B.

Claim 21 has been amended as requested by the Examiner to better claim the idea shown in Figure 6B.

During the interview, the Examiner stated to Applicant's representative that support for claim 5 could not be found in the drawings or the specification. Applicants respectfully disagree because support for claim 5 is present in the drawings in Figures 4A, 4B, 4C, 6A and 6B and in

the specification on pages 18, 19, 20, and 22. Claim 5 recites "The digital processing system of Claim 1, wherein the second instruction is executed before executing the first instruction." A first branch instruction has five delay slots as shown in Table 6 during which other instructions may be executed. The pipeline stages as shown in Table 5 include execute stages E1-E5. Execution of the branch instruction starts at the branch instruction's execute stage E1 and ends at the execute stage E1 of the branch target instruction. Thus, execution of the branch instruction is complete at the execute stage E1 of the branch target instruction. As described on page 22, lines 3-17, the second instruction that is the ADDKPC instruction shown in Figures 6A or 6B is executed in a delay slot of the branch instruction before execution of the branch instruction, i.e. a branch instruction is considered executed at the start of execution of the branch target instruction. Thus, the second ADDKPC instruction is executed before executing the first branch instruction.

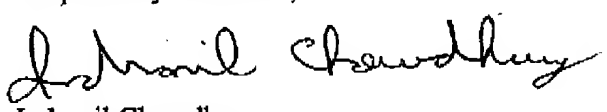
The "Summary of the Invention" section in the specification has been amended on page 5, lines 15-20 to add the subject matter of claim 5. No new matter has been introduced.

The Examiner during the interview pointed out a minor grammar mistake on page 22, line 7. Applicants respectfully suggest that this mistake was already corrected in page 7 of "Response to Office Action Mailed October 19, 2003."

The Examiner during the interview further requested that Figure 1 containing an empty box without a label connected to output 80 should be removed. Applicants have removed the empty box without a label connected to output 80 in Figure 1.

In view of these remarks and amendments, Applicants submit that this application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees and/or credit any overpayment to Deposit Account 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,



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Attachments